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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/693,044	10/20/2000	Yoshihiro Okada	49941(868)	8505
21874	7590	12/08/2003	EXAMINER	
EDWARDS & ANGELL, LLP			PIZIALI, JEFFREY J	
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BOSTON, MA 02209			2673	16

DATE MAILED: 12/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/693,044	OKADA ET AL.
Examiner	Art Unit	
Jeff Piziali	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 21 November 2003.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1,2,4,5,7,8,10-13,19 and 20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1,2,4,5,7,8,10-13,19 and 20 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 12 September 2003 is/are: a) accepted or b) objected to by the Examiner.

 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

 1. Certified copies of the priority documents have been received.

 2. Certified copies of the priority documents have been received in Application No. _____.

 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

 a) The translation of the foreign language provisional application has been received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) Notice of References Cited (PTO-892) 4) Interview Summary (PTO-413) Paper No(s). _____ .

2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) Notice of Informal Patent Application (PTO-152)

3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ . 6) Other: _____ .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 21 November 2003 has been entered.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Election/Restrictions

3. Claims 3, 6, 9, and 14-18 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention and species, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 4 (filed 26 September 2002), and confirmed most recently in Paper No. 15 (filed 21 November 2003).

4. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the

application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Drawings

5. The drawings were received on 12 September 2003. These drawings are acceptable.

Claim Rejections - 35 USC § 102(b)

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1, 4, 7, 10, 19, and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Takeda et al. (US 5,398,043).

Regarding claim 1, Takeda discloses an active-matrix liquid crystal display apparatus comprising: an active-matrix substrate including a plurality of scanning electrode lines [Fig. 1, 1], a plurality of data electrode lines [Fig. 1, 2], pixel electrodes [Fig. 1, A] and switching elements [Fig. 1, 3], the pixel electrodes being respectively connected to intersections of the plurality of scanning electrode lines and the plurality of data electrode lines via the switching elements; a counter electrode substrate including a counter electrode formed thereon, the counter electrode being opposed to the pixel electrodes; a liquid crystal [Fig. 1, 7] sandwiched between the active matrix substrate and the counter electrode substrate; the active-matrix substrate further including supplementary capacitance lines which are formed in parallel to the scanning electrode

lines, and supplementary capacitances [Fig. 1, 8] for holding display data which are connected between the pixel electrodes and the supplementary capacitance lines, the apparatus further comprising: a supplementary capacitance drive circuit [Fig. 1, Ve] for driving the supplementary capacitance lines so that a predetermined potential difference between the voltage applied to the counter electrode and the voltage applied to the pixel electrodes is always maintained when any of the pixel electrodes and supplementary capacitances leaks (see Column 6, Line 21 - Column 8, Line 50).

Regarding claim 4, Takeda discloses the supplementary capacitance lines [Fig. 4, 17] are separated from every scanning electrode line [Fig. 4, 15] to which the switching element for switching driving a pixel potential difference connected through the supplementary capacitance is connected at the intersection, and the supplementary capacitance drive circuit [Fig. 4, 13] drives the supplementary capacitance lines with a polarity being reversed every time an on-signal is input to the scanning electrode line driven at a stage preceding the scanning electrode line (see Fig. 5c; Column 8, Line 55 - Column 9, Line 40).

Regarding claim 7, Takeda discloses the switching element and the pixel electrode are disconnected from each other at a pixel where the leakage between the pixel electrode and the supplementary capacitance line occurs (see Figs. 2 & 5; Column 9, Line 1 - Column 10, Line 12).

Regarding claim 10, this claim is rejected by the reasoning applied in the above rejection of claim 7.

Regarding claim 19, this claim is rejected by the reasoning applied in the above rejection of claim 1.

Regarding claim 20, this claim is rejected by the reasoning applied in the above rejection of claim 1; furthermore, Takeda discloses a supplemental capacitance drive circuit [Fig. 1, 8] including a reference input maintained at the same potential as that of the common electrode for driving the supplemental capacitance lines so that a predetermined potential difference between the voltage [Fig. 1, Vs] applied to the counter electrode [Fig. 1, 7] and the voltages applied to the pixel electrodes is always maintained when any of the pixel electrodes and supplemental capacitances leaks (see Column 6, Line 21 - Column 8, Line 50).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 2, 5, 8, and 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takeda et al. (US 5,398,043).

Regarding claim 2, Takeda discloses a display mode of the LCD apparatus is normally black (see Fig. 3; Column 9, Lines 41-58) and the supplementary capacitance drive circuit drives the supplementary capacitance so that a potential difference not less than a threshold voltage of the liquid crystal is maintained between the pixel electrodes and the counter electrode (see Column 8, Lines 12-34). Takeda does not expressly disclose a display mode of the LCD apparatus being normally white. However, normally-white LCDs were well known and commonly understood at the time of invention. Therefore, it would have been obvious to one skilled in the art at the time of invention to use a normally-white type liquid crystal apparatus as Takeda's LCD, so as to provide energy savings for a image display device that will oftentimes reside in a mainly white state.

Regarding claim 5, this claim is rejected by the reasoning applied in the above rejection of claim 4.

Regarding claim 8, this claim is rejected by the reasoning applied in the above rejection of claim 7.

Regarding claim 11, this claim is rejected by the reasoning applied in the above rejection of claims 1 and 2.

Regarding claim 12, this claim is rejected by the reasoning applied in the above rejection of claim 4.

Regarding claim 13, this claim is rejected by the reasoning applied in the above rejection of claim 7.

Claim Rejections - 35 USC § 102(a)

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

11. Claims 1, 2, 4, 5, 7, 8, 10-13, 19, and 20 are further rejected under 35 U.S.C. 102(a) as being anticipated by Applicants' own admitted prior art.

Regarding claim 1, Applicants' own admitted prior art discloses an active-matrix liquid crystal display apparatus [Fig. 7, 1] comprising: an active-matrix substrate [Fig. 7, 2] including a plurality of scanning electrode lines [Fig. 8, 11], a plurality of data electrode lines [Fig. 8, 12], pixel electrodes [Fig. 8, 14] and switching elements [Fig. 8, 10], the pixel electrodes being respectively connected to intersections of the plurality of scanning electrode lines and the plurality of data electrode lines via the switching elements; a counter electrode substrate [Fig. 7, 3] including a counter electrode [Fig. 8, 16] formed thereon, the counter electrode being opposed to the pixel electrodes; a liquid crystal [Fig. 8, C_{LC}] sandwiched between the active matrix substrate and the counter electrode substrate; the active-matrix substrate further including supplementary capacitance lines [Fig. 8, 15] which are formed in parallel to the scanning electrode lines, and supplementary capacitances [Fig. 8, C_s] for holding display data which are

connected between the pixel electrodes and the supplementary capacitance lines, the apparatus further comprising: a supplementary capacitance drive circuit [Fig. 8, Cs] for driving the supplementary capacitance lines so that a predetermined potential difference between the voltage applied to the counter electrode and the voltage applied to the pixel electrodes is always maintained [wherein, the amount that remains after Vcom is subtracted from VCs is always equal to zero] when any of the pixel electrodes and supplementary capacitances leaks (see Figs. 7-9 and Pages 1-6).

Regarding claim 2, Applicants' own admitted prior art discloses a display mode of the LCD apparatus is normally white (see Fig. 10A) and the supplementary capacitance drive circuit drives the supplementary capacitance so that a potential difference not less than a threshold voltage of the liquid crystal is maintained between the pixel electrodes and the counter electrode (see Pages 7-9).

Regarding claim 4, Applicants' own admitted prior art discloses the supplementary capacitance lines [Fig. 8, 15] are separated from every scanning electrode line [Fig. 8, 11] to which the switching element for switching driving a pixel potential difference connected through the supplementary capacitance is connected at the intersection, and the supplementary capacitance drive circuit [Fig. 8, Cs] drives the supplementary capacitance lines with a polarity being reversed every time an on-signal is input to the scanning electrode line driven at a stage preceding the scanning electrode line (see Figs. 7-9 and Pages 1-6).

Regarding claim 5, this claim is rejected by the reasoning applied in the above 102(a) rejection of claim 4.

Regarding claim 7, Applicants' own admitted prior art discloses the switching element and the pixel electrode are disconnected from each other at a pixel where the leakage between the pixel electrode and the supplementary capacitance line occurs (see Figs. 7-9 and Pages 1-6).

Regarding claim 8, this claim is rejected by the reasoning applied in the above 102(a) rejection of claim 7.

Regarding claim 10, this claim is rejected by the reasoning applied in the above 102(a) rejection of claim 7.

Regarding claim 11, this claim is rejected by the reasoning applied in the above 102(a) rejection of claims 1 and 2.

Regarding claim 12, this claim is rejected by the reasoning applied in the above 102(a) rejection of claim 4.

Regarding claim 13, this claim is rejected by the reasoning applied in the above 102(a) rejection of claim 7.

Regarding claim 19, this claim is rejected by the reasoning applied in the above 102(a) rejection of claim 1.

Regarding claim 20, this claim is rejected by the reasoning applied in the above 102(a) rejection of claim 1; furthermore, Applicants' own admitted prior art discloses a supplementary capacitance drive circuit [Fig. 8, Cs] including a reference input [Fig. 8, i.e. the unlabeled line inputting 16 to 13] maintained at the same potential as that of the common electrode for driving the supplemental capacitance lines so that a predetermined potential difference [wherein, the amount that remains after Vcom is subtracted from Vc_s is always equal to zero] between the voltage applied to the counter electrode and the voltages applied to the pixel electrodes is always maintained when any of the pixel electrodes and supplemental capacitances leaks (see Figs. 7-9 and Pages 1-6).

Response to Arguments

12. Applicants' arguments filed 21 November 2003 have been fully considered but they are not persuasive. Firstly, the Applicants contend the cited prior art of Takeda et al. (US 5,398,043) fails to disclose a predetermined potential difference between the voltage applied to the counter electrode and the voltage applied to the pixel electrodes is always maintained when any of the pixel electrodes and supplementary capacitances leaks. However, the examiner respectfully disagrees. Takeda explicitly discloses, "the potential fluctuation ΔV which appears at the pixel electrode can be so controlled as to be a desired value by controlling Ve(+) and Ve(-)" (see Column 8, Lines 15-18). Thereby, Takeda teaches a predetermined potential difference between

the voltage applied to the counter electrode and the voltage applied to the pixel electrodes is always maintained when any of the pixel electrodes and supplementary capacitances leaks.

Secondly, the Applicants contend the instant application's own admitted prior art fails to teach a supplementary capacitance drive circuit including a reference input maintained at the same potential as that of the common electrode for driving the supplemental capacitance lines so that a predetermined potential difference between the voltage applied to the counter electrode and the voltages applied to the pixel electrodes is always maintained when any of the pixel electrodes and supplemental capacitances leaks. However, the examiner again respectfully disagrees. The Applicants' own admitted prior art explicitly discloses a supplementary capacitance drive circuit [Fig. 8, Cs] including a reference input [Fig. 8, i.e. the unlabeled line inputting 16 to 13] maintained at the same potential as that of the common electrode for driving the supplemental capacitance lines so that a predetermined potential difference [wherein, the amount that remains after V_{com} is subtracted from V_{Cs} is always equal to zero] between the voltage applied to the counter electrode and the voltages applied to the pixel electrodes is always maintained when any of the pixel electrodes and supplemental capacitances leaks (see Figs. 7-9 and Pages 1-6). By such reasoning, rejection of the claims is deemed proper, necessary, and thereby maintained at this time.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Piziali whose telephone number is (703) 305-8382. The examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on (703) 305-4938. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9314.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4700.



J.P.
5 December 2003



BIPIN SHALWALA
SUPERVISED PATENT EXAMINER
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